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<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/669,427	ITAKURA, KATSUHIKO	
	<b>Examiner</b>	<b>Art Unit</b>	
	Toan Le	2824	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to \_\_\_\_\_.
2. ☒ The allowed claim(s) is/are 1-21.
3. ☒ The drawings filed on 25 September 2003 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☒ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☒ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
  - \* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
  - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |   |  |
|---|--|
| 1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 6. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date _____. |
| 3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br>Paper No./Mail Date <u>9/25/03</u> | 7. <input type="checkbox"/> Examiner's Amendment/Comment                               |
| 4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material                              | 8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance   |
|   | 9. <input checked="" type="checkbox"/> Other <u>East search history</u> .              |

*Handwritten signature and date 6/13/05*

**RICHARD ELMS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800**

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. This office acknowledge receipt of the following items from the Applicant:  
Information Disclosure Statement (IDS) filed on September 25, 2003.
2. Information disclosed and list on PTO 1449 was considered.

### ***Allowable Subject Matter***

3. Claims 1-21 are allowable over the art of record.
4. The following is an examiner's statement of reasons for allowance: There is no suggestion or teaching in the art of record to provide a semiconductor integrated circuit device or a self-test method of memory macro built in a semiconductor integrated circuit device comprising a physical row region or a physical column region is allocated to respective a logical row region or a logical column region by an allocating section, in combination with the remaining claimed limitation as recited in the independent claims 1 and 18, nor is there suggestion or teaching to provide a frequency controlling section for converting a clock signal supplied from an external section into an internal clock signal that is a maximum frequency when the memory macro is at the time of the test, in combination with the remaining claimed limitation as recited in the independent claims 4 and 19, nor is there suggestion or teaching to provide a latency-value storing section for storing a latency-value information which is supplied by a set-latency-value switching section in self-test, in combination with the remaining claimed limitation as recited in the independent claims 9 and 20, nor is there suggestion or teaching to

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provide an output latency controlling section for controlling output latency depending on propagation delay time and operation frequency of a clock signal through an output path from a defective region storing section, in combination with the remaining claimed limitation as recited in the independent claims 15 and 21.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ishikawa (U.S. 6,711,042) discloses a logic chip comprising a logic circuit having prescribed functions and a memory chip testing circuit for performing operation test on a memory chip.

Zuraski, Jr. et al. (U.S. 6,560,740) disclose an apparatus and method for programmable built-in self-test and built-in self-repair of an embedded memory.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Le whose telephone number is (571) 272-1872. The examiner can normally be reached on M-F (8.00AM - 5.30PM).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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June 12, 2005